## IN THE CLAIMS

Please amend claims 4, 8, 12, and 16 and add claims 17, 18, and 19 as follows:

4 (Amended). A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of series connected MOS transistors wherein at least one of said plurality of series connected MOS transistors is a NMOS transistor, at least one of said plurality of series connected MOS transistors is a PMOS transistor, and at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body ;

a precharge circuit connected to a clock signal, a circuit supply voltage, and said pull-down network;

a ground switch circuit connected to said clock signal and to said pull-down network; and

an output node which is connected to a common node of said pull-down network and said precharge circuit.

8 (Amended). A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of series connected PMOS transistors wherein at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body ;

a precharge circuit connected to a clock signal, a circuit supply voltage, and said pull-down network;

a ground switch circuit connected to said clock signal and to said pull-down network; and

an output node which is connected to a common node of said pull-down network and said precharge circuit.

12 (Amended). A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected MOS transistors with a first and second common node, wherein at least one of said plurality of parallel connected MOS transistors is a NMOS transistor, at least one of said plurality of parallel connected MOS transistors is a PMOS transistor, and at least one of said MOS transistors in said pull-down network has a gate tied to a floating substrate body ;

a precharge circuit connected to a clock signal and to said first common node of said pull-down network;

a ground switch circuit connected to said clock signal and to said second common node of said pull-down network; and

an output node which is connected to said first common node of said pull-down network.

16 (Amended). A dynamic logic circuit on a SOI substrate, comprising:

a pull-down network comprising a plurality of parallel connected PMOS transistors with a first and second common node wherein at least one of said PMOS transistors in said pull-down network has a gate tied to a floating substrate body ;

a precharge circuit connected to a clock signal and to said first common node of said pull-down network;

a ground switch circuit connected to said clock signal and to said second common node of said pull-down network; and

an output node connected to said first common node of said pull-down network.

17. A logic circuit, comprising:

providing a silicon on insulator semiconductor;

a NMOS transistor formed in said silicon on insulator semiconductor with a n-type source/drain region;

a PMOS transistor formed in said silicon on insulator semiconductor with a p-type source/drain region wherein said p-type source/drain region of said PMOS transistor abuts said n-type source/drain region of said NMOS transistor.

18. The logic circuit of claim 17 wherein said NMOS transistor further comprises a gate tied to a floating substrate body.

19. The logic circuit of claim 17 wherein said PMOS transistor further comprises a gate tied to a floating substrate body.